CO 639 — Quantum Error Correcting Codes
Proving the Threshhold theorem

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1 Definitions

We'll start by recapping what we wish to prove, and the relevant definitions.

Threshold Theorem. *Let p be the error rate per gate (or per time-step) in a quantum circuit, and ε be the error rate per gate (or per time-step) that we wish to achieve. Then, there is a threshold p_c such that if $p < p_c$, we can perform an arbitrary quantum computation using* $\mathrm{poly}(\log \varepsilon)$ *overhead per logical gate (or per time-step).*

Definition 1. Error correction structures and units:

- A *level* 0 *block* is a single qubit.
- A *level* l *block* is seven level $(l-1)$ blocks (i.e. 7^l qubits)
- A *level* 0 *rectangle* is a single physical gate.
- A *level* l *gate rectangle* is a transversal operation made of level $(l-1)$ rectangles operating on level $(l-1)$ blocks, preceded and followed by level $(l-1)$ error-correction steps on each level $(l-1)$ block.
- A *level* l *input rectangle* consists of level $(l-1)$ error-correction on the level $(l-1)$ blocks within a level l block, before any level l gate rectangles are performed on that level l block.
- A *level* l *output rectangle* consists of level $(l-1)$ error-correction on the level $(l-1)$ blocks within a level l block, performed after any level l gate rectangles which have been performed on that level l block.
- A *level* l *ancilla preparation rectangle* is a rectangle containing the encoding circuits producing a number of level l encoded states out of level $l-1$ encoded states, and testing the ancillas to produce one reliable level l ancilla.

Let us also add:

- A *level* l *circuit* is the union of a sequence of level l gate rectangles.

- The *input rectangles* to a level l circuit are the first input rectangles involving each level l block acted on by the circuit.
- The *output rectangles* of a level l circuit are the last output rectangles involving each level l block acted on by the circuit.
- *Level l error correction* (or EC) is a level l circuit designed to circuit errors in level l subblocks of a level $(l+1)$ block.

Definition 2. Error correction states and situations:

- A level 0 rectangle is *bad* if the gate has an error.
- A level l gate rectangle is *bad* if it contains two or more bad level $(l-1)$ sub-rectangles or if one of its level l ancilla rectangles is bad.
- A level l block becomes *bad* if it is operated on by a bad rectangle, it interacts with another block which has become bad, or it has two or more bad sub-blocks.
- A level l block becomes *good* if it experiences level l error correction involving no bad level l rectangles.
- A level l ancilla preparation rectangle is *bad* if it produces a bad level l block.
- A level l input (or output) rectangle is *bad* if

  i. the input state is a bad level l block;

  ii. the number of bad level $(l-1)$ input sub-rectangles, plus the number of bad level $(l-1)$ gate sub-rectangles, is greater than 1.

  In both cases, we should include the ancillas used for error correction to be among the input states to the rectangle.

We can use these definitions, and tie them into our goal, through one final definition:

Definition 3. The *ideal decoding operation* is the decoding operation that would be performed by circuit with no errors at all in it. A circuit for a unitary operation U is *correct* if it performs an encoded U operation on the encoded input state provided to it (whether the block it operates upon is good or bad). Namely, a correct circuit for U followed by ideal decoding produces the same state as ideal decoding followed by U.

Since the ideal decoding operation has the ability to correct one error in a block, a circuit can be correct even if it has an error (e.g., a bad subrectangle).

The way which we will prove the Threshold theorem is by matching up the concepts of good rectangles with correct circuits.

Theorem 1 ("good = correct").

1. *A good level l ancilla preparation rectangle produces a good level l block encoding the state $|0\rangle$. (I.e., ideal decoding produces the state $|0\rangle$.)*
2. *Suppose that a level l circuit has only good level l gate rectangles, and only good level l ancilla preparation rectangles.*

- *If all the circuit's input rectangles are good, then the circuit is correct.*
- *If some of the circuit's input rectangles are bad, then the circuit acts correctly as if errors were potentially present on the bad input rectangles.*

Proof (by induction) — The case for $l = 0$ is trivial. For the induction step, suppose that the Theorem holds for some particular value of $l \in \mathbb{N}$, and suppose further that we have a level $(l+1)$ circuit C. The level $(l+1)$ circuit is composed of a number of level l subrectangles, and we know by induction that the good subrectangles behave correctly; we can thus treat them as level 0 gates, and our level $(l+1)$ circuit as a level 1 circuit composed of level 0 gates, some of which may have errors in them. More specifically:

- Suppose that C is a circuit composed of a number of good gate rectangles.

  Claim: If C is good, and its input and ancilla preparation sub-rectangles are good, then its output rectangles are good as well.

  To prove this claim, suppose that C, as well as its input/ancilla preparation rectangles, are indeed all good. We will prove it when C is a single gate rectangle, in which case the claim will follow by putting together the result for all the gate rectangles in the circuit.

  - If the input state to an input rectangle has one bad sub-block, this will be corrected by the error correction (as it can have no bad sub-rectangles if the input rectangle is good).
  - If an input rectangle has one bad sub-rectangle, then the output of that rectangle will have one bad level l sub-block, but will be good at level $l+1$. The gate part and output rectangles can have no bad gate sub-rectangles, as C is good, so the output rectangles are good.
  - If there is a bad sub-rectangle later in the gate rectangle — in the gate part or one of the output rectangles — then there can be no bad gate sub-rectangles in any of the input rectangles, so that the state after the input rectangles will be all good at level l. There can be at most one bad subrectangle in the output rectangles, so they are all good.
  - If there are no bad subrectangles anywhere in C, everything is alright.

  Based on this claim, it is sufficient to consider gate rectangles one at a time, as "goodness" and "badness" propagate just the way errors do.

- Suppose that C is a single good gate rectangle which has only good level $l+1$ input rectangles. Consider first the initial level l EC step performed by a single such input rectangle. This EC circuit consists of a number of level l gate subrectangles, and has input rectangles of its own. As the EC step makes up a level $l+1$ input rectangle, one of the level l gate rectangles in this EC step can be bad, or one of its level l input rectangles can be bad, but not both.

  - If one of the level l input rectangles is bad, we may apply the Theorem at level l, and see that the EC circuit corrects any error on the subblock of the bad rectangle. In this case, the state exiting the EC is correct at level l (although it may have bad level $l-1$ subblocks): then, an ideal decoding performed at level l would give us a correct codeword, encoding the state that ideal decoding at level $l+1$ would have produced before the EC step. From the preceding case, the level l output rectangles of the level l EC step are all good.
  - If one of the gate subrectangles is bad, we consider only the gate subrectangles acting on the other level l subblocks. Since they are all good, and their level l input rectangles are all good, the induction hypothesis implies that the circuit acts correctly on all the blocks

except for the one with the bad gate subrectangle, and blocks which interact with it after that rectangle. Since the EC step is fault-tolerant, the block exiting the EC step has only one error at level l in the affected subblock; all the other level l output rectangles are good. An ideal decoding performed at level l would give us a correct codeword, encoding the state that ideal decoding at level $l+1$ would have produced before the EC step.

Now, consider the remainder of the circuit C. As C is good, it can have at most one bad subrectangle.

- Suppose one of the input rectangles has a bad subrectangle. Then, there are no bad subrectangles in the rest of C. The theorem applied to level l says the rest of the circuit acts correctly, and since it is fault-tolerant, the error that may be left over from the initial EC steps cannot spread to a different block, and is corrected by the EC steps in the output rectangles of C. Level $l+1$ ideal decoding therefore produces the correct state.
- Suppose there is a bad level l gate later in the circuit C. We treat this just as we did an error in the input EC steps, by ignoring the block it affects. The other level l subblocks experience only good level l gate subrectangles, and therefore the level l circuit acts correctly on them. Since the circuit is fault-tolerant, the error cannot spread, and the other blocks behave correctly. Again, level $l+1$ ideal decoding produces the correct state.

Then, the result is shown for a good gate rectangle with only good input rectangles.

- Now suppose C is a single good gate rectangle, but it has one or more bad level $l+1$ input rectangles. Again we consider the input EC stages as circuits of level l gates. Since C is good, there can be at most one bad level l gate subrectangle in all of the EC circuits.
  - Consider first an EC circuit that has no bad gate subrectangles, but is part of a bad input rectangle nonetheless. That is, the input block to the rectangle is a bad level $l+1$ block (possibly also with bad level l input blocks). By the induction hypothesis, this EC step corrects level l errors producing a state which decodes at level l to a state in the level $l+1$ code; however, it is an erroneous codeword, as the level $l+1$ input state is bad.
  - Next, consider the case of an EC circuit with one bad level l gate subrectangle which is part of a bad level $l+1$ input rectangle. In this case, the state after EC is likely to be bad at level $l+1$, and could also have an error at level l (under level l ideal decoding). Note, however, that at most one of the EC circuits can have a bad level l gate subrectangle, as they are all part of the same good level $l+1$ rectangle C. Therefore, if we consider the state under ideal level l decoding just before the gate part of C, we get a state that has at most one level l error (but may have errors at level $l+1$ wherever the level $l+1$ input rectangles were bad). Thus, the remainder of the circuit will act correctly on this state: in particular, any preexisting level $l+1$ errors will be propagated or not propagated as appropriate to their type and the gate being performed.

  Then, the theorem is correct for a good gate rectangle with some bad input rectangles.

- Suppose that C is a good ancilla preparation rectangle, meaning the state it produces is good. We have defined "badness" so it propagates just the way errors do under ideal level l decoding (as a consequence of the theorem applied at level l). Therefore, the good level $l+1$ ancilla state, which has at most one bad level l subblock, encodes a $|0\rangle$ state under level $l+1$ ideal decoding.

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The probability of an error in a level l gate will be the probability that one of its rectangles is bad (either a gate rectangle or an ancilla preparation rectangle).

A bad gate rectangle has at least two bad sub-rectangles: if the probability of a bad gate rectangle at level l is p_l , then we have

$$p_l = \binom{N}{2} {p_{(l-1)}}^2$$

where N is the number of subrectangles in total. A bad ancilla preparation rectangle at level l also has at least 2 bad sub-rectangles, which will also occur with probability on the order of $O({p_{(l-1)}}^2)$. Then, the threshhold probability p_c at which error correction will allow us to reduce the effective error rate will be

$$p_c \sim \frac{1}{\binom{N}{2}} \approx 10^{-6}$$

where N is an upper bound on the number of sub-rectangles in a level l rectangle.